

REMARKS

Claims 7-26 are pending in the current application. Claims 7-26 were previously presented in a Preliminary Amendment. Claims 1-6 were previously canceled. Claims 7, 14, and 21 are currently amended.

The Office Action indicates that claims 7-26 are rejected.

Applicants respectfully request reconsideration of the application in view of the foregoing amendments and the remarks appearing below.

Rejections under 35 U.S.C. §103

Irrinki et al./Park et al.

Claims 7, 9-13, 14, 16-23, 25-26 stand rejected under 35 U.S.C. §103(a) as being obvious in view of a combination of U.S. Patent No. 5,987,632 to Irrinki et al. and U.S. Patent No. 6,574,757 to Park et al.. Applicants respectfully disagree.

Irrinki et al. disclose a two-pass test for making row and column repairs to a memory using redundant elements. The first pass involves testing a memory element under worst case conditions and, if a failure is seen, marking it as permanently failing. The second pass is performed under more normal operating conditions and involves rediscovering the memory element marked as failing in the first pass and mapping a redundant memory element as a replacement (along with repairing/mapping redundant elements to repair any newly found fails). Importantly, Irrinki et al. are completely silent on the use of any sort of weighting scheme and a third memory element for accumulating failed row and column addresses and associated assigned weights.

Park et al. disclose an integrated redundancy architecture for providing BIST redundancy allocation to an embedded memory system. The Park et al. architecture includes 1) a BIST for identifying and transmitting row and column addresses from failed memory, 2) a first memory element (Fig. 4A) for accumulating the row addresses of failed memory cells, a row weight and column fill entry pointers to the corresponding column address in the second memory element, 3) a second memory element (Fig. 4B) for accumulating column addresses of failed memory cells, a column weight, and row fill entry pointers to the corresponding row address in the first memory element, and 4) means for allocating redundancy (Fig 10A-11B) to rows and/or columns containing failed memory cells based upon the number of fill entry pointers occupied (col. 10,

line 62- col. 11, line 13) and the relative magnitudes of the row weights or column weights, which allocates all of redundant rows or all of the redundant columns first, depending upon which is the major entry and which is the minor entry (col. 11, lines 39-47). Thus, Park et al. teaches a BIST to find bad memory addresses, splitting the bad memory address information into row and column components stored in two separate memory elements, yet with cross-referencing "pointers" linking the two separate memory elements, and a method for generating row or column weights for each row or column containing failed memory. Because of the limited space for cross-reference pointers, repairs using redundancy must begin when the pointer storage is filled for any individual row or column. This will generally force repairs before all failed memory has been found.

Turning now to the rejected claims, independent claim 7, as amended, requires the limitations of 1) "a third memory element for accumulating ones of the row and column addresses not already contained in said first and second memory elements and for assigning each of the failed row and column addresses a particular weight value based on the number of the failed row and column addresses already accumulated in said third memory element and the relative locations of the failed row and column addresses within the memory system," and 2) "means for determining whether the row address of a failed memory cell matches any of the to-be-repaired row addresses stored in the first memory element; determining whether the column address of the failed memory cell matches any of the to-be-repaired column addresses stored in the second memory element; if the row address of the failed memory cell does not match any of the to-be-repaired row addresses stored in the first memory element and the column address of the failed memory cell does not match any of the to-be-repaired column addresses stored in the second memory element, storing the row and column addresses of the failed memory cell in the third memory element; if either the row address of the failed memory cell matches one of the to-be-repaired row addresses stored in the first memory element or the column address of the failed memory cell matches one of the to-be-repaired column addresses stored in the second memory element, or both, then: determining whether the row address of another failed memory cell matches any of the to-be-repaired row addresses stored in the first memory element; and determining whether the column address of the another failed memory cell matches any of the to-be-repaired column addresses stored in the second memory element." Support for these amendments is found in the current application in FIG. 2 and in the written

description at ¶0016. These limitations are directed to a redundancy allocation scheme that is very different from the scheme that Park et al. teach. Consequently, Park et al. fail to disclose or suggest at least the novel means of amended claim 7. For at least this reason, Applicants respectfully submit that the applied combination of the Irrinki et al. and Park et al. patents neither discloses nor suggests amended independent claim 7, nor claims 9-13 that depend therefrom.

Regarding currently amended independent claim 14, this claim requires among other things the limitation of “reducing the corresponding row or column weight values of the remaining failed row and column addresses in the third memory element that share defective memory addresses with the repaired rows or columns.”

Applicants respectfully submit that neither the Irrinki et al. patent nor the Park et al. patent discloses or suggests this limitation. Again, the weighting methodology of Park et al. is much different and does not involve reducing of weights in the manner claimed. For at least this reason, Applicants respectfully submit that the applied combination of the Irrinki et al. and Park et al. patents cannot render obvious amended independent claim 14, nor claims 16-20 that depend therefrom.

Regarding amended independent claim 21, this claim requires among other things the identical means-for limitation as found in amended claim 7. Thus, for at least the same reasons as discussed above relative to amended claim 7, Applicants respectfully submit that the applied combination of the Irrinki et al. and Park et al. patents cannot render obvious amended independent claim 21, nor claims 22-26 that depend therefrom.

In view of the foregoing, Applicants respectfully request withdrawal of the present rejection.

Irrinki et al./Park et al./Ohtani et al.

Claims 8, 15 and 24 stand rejected under 35 U.S.C. §103(a) as being obvious in view of a combination of the Irrinki et al. and Park et al. patents, discussed above, and further in view of U.S. Patent Application Publication 2002/0196683 A1 to Ohtani et al.. Applicants respectfully disagree.

In light of the amendments to claims 7, 14 and 21, from which claims 8, 15 and 24 respectively depend, Applicants believe that the dependent claims 8, 15 and 24 are now allowable. The amendments add the limitations discussed above with regard to claims 7, 14 and 21 that are neither taught nor suggested by the Irrinki et al./Park et al. combination. Since

the Ohtani et al. publication also fails to teach or suggest these limitations, the addition of the Ohtani et al. publication to the Irrinki et al./Park et al. combination does not provide the limitations of amended independent claims 7, 14 and 21 missing from the Irrinki et al./Park et al. combination. Therefore, these claims, as well as dependent claims 8, 15 and 21 are patentable over the Irrinki et al./Park et al./Ohtani et al. combination.

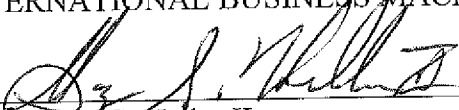
In view of the foregoing, Applicants respectfully request withdrawal of the present rejection.

CONCLUSION

In view of the foregoing, Applicants respectfully submit that claims 7-26, as amended, are in condition for allowance. If any issues remain, the Examiner is encouraged to call the undersigned attorney at the number listed below.

Respectfully submitted,

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